AMENDMENTS TO CLAIMS

1. (original) A circuit for calculating and outputting a modulo value resulting from a simulated division of a dividend by a divisor, the circuit comprising:

a plurality of subtraction circuits, each one of the subtraction circuits receiving as a first input a common dividend signal representing the dividend and, as a second input, at least one respective test value signal representing a respective integer multiple of the divisor, each one of the subtraction circuits subtracting the respective test value signal input to the subtraction circuit from the common dividend signal to produce a respective remainder signal and a respective carry/borrow signal; and

logic coupled to receive each of the corresponding carry/borrow signals and to determine therefrom which of the remainder signals represents a true remainder of the division of the dividend by the divisor.

2. (original) The circuit recited in claim 1, further comprising a multiplexer that receives each of the remainder signals and, in response to a signal from said logic, outputs the remainder signal representing the true remainder of the division operation.

3. (original) The circuit of claim 1, wherein the plurality of subtraction circuits execute the respective subtraction operations substantially simultaneously.

4. (original) The circuit of claim 1, wherein the respective test value signals are hard coded in the circuit.

5. (original) The circuit of claim 1, wherein each one of the subtraction circuits receives as its second input, at least a further test value signal representing a further integer multiple of the divisor, and wherein each one of the subtraction circuits subtracts the test value signal from the dividend signal during a first subtraction operation and subtracts the further test value signal from the dividend signal during a second subtraction operation.

6. (original) The circuit of claim 1, wherein the plurality of subtraction circuits is used during a first subtraction cycle to perform respective subtractions using a first subset of respective test value signals, and wherein the plurality of subtraction circuits is then reused during a second subtraction cycle to perform respective subtractions using a second subset of respective test value signals.

7. (original) The circuit recited in claim 6, further comprising a sequence controller that controls the input of the first and second subsets of test value signals to the subtraction circuits during the respective first and second subtraction cycles.

8. (original) The circuit recited in claim 1, wherein the dividend comprises a variable dividend having a value ranging from 0 to 65535 inclusive, and wherein the divisor comprises a fixed value of 9973.

9. (original) The circuit recited in claim 1, wherein each subtraction circuit comprises an adder that receives as its first input the common dividend signal and as its second input a two's complement form of said at least one respective test value signal, and wherein each adder performs its respective subtraction operation using two's complement arithmetic.

10. (original) The circuit recited in claim 1, wherein the respective test value signals are available as inputs to each subtraction circuit prior to each subtraction circuit receiving said common dividend signal.

11. (original) The circuit recited in claim 1, wherein the respective test value signals are available as inputs to each subtraction circuit substantially simultaneously with each subtraction circuit receiving said common dividend signal.

Claims 12-14 (canceled).

15. (new) A method performed by data processing apparatus for compressing an input data stream represented by a plurality of electrical signals, said method comprising:

processing said input data stream to produce index values based upon byte string values from said input data stream, each of said index values being represented by a respective dividend signal;

providing a divisor signal having a fixed value;

performing a simulated modulo division of each dividend signal by said divisor signal comprising the steps of:

providing a plurality of test value signals each representing a different integer multiple of said divisor signal;

for each dividend signal resulting from said processing, applying the dividend signal along with said test value signals to subtraction means for separately subtracting each test value signal from the dividend signal so as to produce a respective remainder signal and a respective carry/borrow signal for each test signal, and

processing said respective remainder signals and said respective carry/borrow signals to determine which of the remainder signals represents a true remainder for the division;

using the determined true remainders to assign locations in a dictionary for storing code words representing said input data stream; and

outputting and assembling code words from said dictionary to produce a compressed representation of said input data stream.

16. (new) The method recited in claim 15, wherein the dividend signal has a variable value ranging from 0 to 65536 inclusive, and wherein the divisor signal comprises a fixed value of 9973.

17. (new) The method recited in claim 15, wherein said subtracting means performs said subtracting for a first subset of test value signals, and thereafter, is used again for performing subtractions for a second subset of test value signals.